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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/827,175	04/06/2001	Michael Sokol	023925-00003	4372

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EXAMINER	
YAO, KWANG BIN	
ART UNIT	**PAPER NUMBER**
2667	

DATE MAILED: 01/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/827,175	SOKOL ET AL.
	Examiner	Art Unit
	Kwang B. Yao	2667

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Erimli et al. (US 6,760,341).

Erimli et al. discloses a network switching system comprising the following features: as depicted in Fig. 2, regarding claim 1, a first switch (22a) having a FIRST MEMORY INTERFACE (44a) and a first expansion port (30); an expansion bus (32) having a first expansion bus (32) interface and a second expansion bus (32) interface, said first expansion bus (32) interface connected to said first expansion port (30); and a second switch having a SECOND MEMORY INTERFACE (44b) and a second expansion port (30), said second expansion port (30) connected to said second expansion bus (32) interface, thereby connecting said first switch (22a) to said second switch (22b), wherein said expansion bus (32) allows said first switch (22a) to directly access said SECOND MEMORY INTERFACE (44b) through said second switch (22b) and said second switch (22b) to directly access said FIRST MEMORY INTERFACE (44a) through said first switch (22a); regarding claim 2, wherein said first expansion port (30) further comprises a first proxy component (28) that enables data packets to

be read from said first memory (36a) and written to said first memory (36a) by said second switch through said expansion bus (32), and wherein said second expansion port (30) further comprises a second proxy component (28) that enables data packets to be read from said second memory (36b) and written to said second memory (36b) by said first switch (22a) through said expansion bus (32); regarding claim 3, wherein said FIRST MEMORY INTERFACE (44a) is configured to be connected to a first external memory (36a, 36b) and said SECOND MEMORY INTERFACE (44b) is configures to be connected to a second external memory (36a, 36b); regarding claim 4, further comprising a command bus (Fig. 2,, REF 38, column 6, lines 9-15) connected between said first switch (22a) and said second switch (22b) allowing commands to be communicated between said first switch (22a) and said second switch (22b); regarding claim 5,a switch for transmitting and receiving data packets comprising: a memory interface that accesses memory; and an expansion port (30) connected to said memory interface, wherein said expansion port (30) is configured to be connected to an expansion bus (32) connected to another switch thereby connecting two switches together allowing for sharing of memory; regarding claim 6, wherein said expansion port (30) further comprises a proxy component (28) that when activated allows data packets to be read from said memory and written to said memory from another switch through said expansion port (30); regarding claim 7, wherein said memory interface is configured to access external memory (36a, 36b); regarding claim 8, further comprising a command bus (Fig. 2,, REF 38, column 6, lines 9-15) interface configured to be connected to another switch allowing commands to be communicated between switches; regarding claim 9, a system of network of switches, said system comprising: a first switch (22a) having a first memory (36a) and a first expansion port (30); an expansion bus (32) having a first

expansion bus (32) end and a second expansion bus (32) end, said first expansion bus (32) end connected to said first expansion port (30); and a second switch (22b) having a second memory (36b) and a second expansion port (30), said second expansion port (30) connected to said second expansion bus (32) end, thereby connecting said first switch (22a) to said second switch (22b), wherein said expansion bus (32) allows said first switch (22a) to directly access said second memory (36b) through said second switch (22b) and said second switch (22b) to directly access said first memory (36a) through said first switch (22a); regarding claim 10, wherein said first expansion port (30) further comprises a first proxy component (28) that when activated allows data packets to be directly read from said first memory (36a) and directly written to said first memory (36a) by said second switch (22b) through said expansion bus (32), and wherein said second expansion port (30) further comprises a second proxy component (28) that when activated allows data packets to be directly read from said second memory (36b) and directly written to said second memory (36b) by said first switch (22a) through said expansion bus (32); regarding claim 11, wherein said first memory (36a) is external memory (36a, 36b) and said second memory (36b) is external memory (36a, 36b); regarding claim 12, further comprising a command bus (Fig. 2,, REF 38, column 6, lines 9-15) connected between said first switch (22a) and said second switch (22b) allowing commands to be communicated between said first switch (22a) and said second switch (22b); regarding claim 13, a method for sharing memory between a first switch (22a) and a second switch (22b) connected to each other by an expansion bus (32) comprising the steps of: sending a command from a first switch (22a) to a second switch (22b) that said first switch (22a) is about to perform a memory read or write; reading or writing a portion of packet data to local memory of said first switch (22a); and reading or writing another

portion of packet data to alternate memory through said second switch (22b) using said expansion bus (32); regarding claim 14, wherein said step of sending a command further comprises configuring said second switch (22b) to be a proxy allowing said packet data to be read from said second memory (36b) or written to said second memory (36b) by said first switch (22a) through said expansion bus (32); regarding claim 15, wherein said step of sending a command comprises the step of sending said command across a command bus (Fig. 2,, REF 38, column 6, lines 9-15) connected between said first switch (22a) and said second switch (22b) allowing commands to be communicated between said first switch (22a) and said second switch (22b). See Abstract, and column 4-6.

Response to Arguments

3. Applicant's arguments filed 11/9/04 have been fully considered but they are not persuasive.

On page 5, first paragraph, Applicant argues that Erimli et al. does not disclose or suggest the feature of an expansion bus allowing the first switch to directly access the second memory interface through the second switch and the second switch to directly access the first memory interface through the first switch. Examiner respectfully disagrees with this argument. It is noted that Erimli et al. discloses the following features: an expansion bus (Fig. 2, bus 32) allowing the first switch (Fig. 2, switch 22a) to directly access the second memory interface (Fig. 2, memory interface 44b) through the second switch (Fig. 2, switch 22b) and the second switch (Fig. 2, switch 22b) to directly access the first memory interface (Fig. 2, memory interface 44a) through the first switch (Fig. 2, switch 22a). See column 2, lines 45-49; column 3, lines 2-15.

On page 5, second paragraph, Applicant argues that Erimli et al. does not disclose the following features: claim 1 recites "said expansion bus allows said first switch to directly access said second memory interface through said second switch and said second switch to directly access said first memory interface through said first switch." Claim 5 recites "an expansion port connected to said memory interface, wherein said expansion port is configured to be connected to an expansion bus connected to another switch, thereby connecting two switches together allowing for sharing of memory." Claim 9 recites some features similar to claim 1, but is directed to a system of network switches. Claim 13 recites "reading and writing another portion of packet data to alternate memory through said second switch using said expansion bus". Examiner respectfully disagrees with these arguments. Erimli et al. discloses the following features: claim 1 recites "said expansion bus (Fig. 2, bus 32) allows said first switch (Fig. 2, switch 22a) to directly access said second memory interface (Fig. 2, memory interface 44b) through said second switch (Fig. 2, switch 22b) and said second switch (Fig. 2, switch 22b) to directly access said first memory interface (Fig. 2, memory interface 44a) through said first switch (Fig. 2, switch 22a)." Claim 5 recites "an expansion port (Fig. 2, port 30) connected to said memory interface (Fig. 2, memory interface 44a), wherein said expansion port (Fig. 2, port 30) is configured to be connected to an expansion bus (Fig. 2, bus 32) connected to another switch, thereby connecting two switches (Fig. 2, switch 22a, 22b) together allowing for sharing of memory." Claim 9 recites some features similar to claim 1, but is directed to a system of network switches (Fig. 2, switch 22a, 22b). Claim 13 recites "reading and writing another portion of packet data (column 5, lines 1-42) to alternate memory (Fig. 2, memory 36b) through said second switch (Fig. 2, switch 22b) using said expansion bus (Fig. 2, bus 32)".

On page 6, first paragraph, Applicant argues that Erimli does not disclose or suggest directly accessing these memories from one switch to another through an expansion bus. For example, Erimli does not disclose or suggest switching module 22a of Figure 2 directly accessing memory interface 44c. Further, Erimli does not disclose or suggest bus 32 of Figure 2 providing access to any memory interface of the switching modules. Examiner respectfully disagrees with these arguments. Erimli et al. discloses the following features: any switch module (22a, 22b, 22c) can access any one of memory device (36a, 36b, 36c); and bus (32) provides access to any memory interface (44a, 44b, 44c) of the switching modules (22a, 22b, 22c). See column 3, lines 2-15; column 5, lines 1-42.

On page 6, second paragraph, Applicant argues that Erimli does not disclose or suggest an expansion bus that allows a first switch to directly access a second memory through a second switch and a second switch to directly access a first memory through the first switch. Examiner respectfully disagrees with these arguments. Erimli et al. discloses the following features: an expansion bus (Fig. 2, bus 32) that allows a first switch (Fig. 2, switch 22a) to directly access a second memory (Fig. 2, memory 36b) through a second switch (Fig. 2, switch 22b) and a second switch (Fig. 2, switch 22b) to directly access a first memory (Fig. 2, memory 36a) through the first switch (Fig. 2, switch 22a).). See column 3, lines 2-15; column 5, lines 1-42.

On page 7, Applicant argues that the dependent claims are allowable because of their dependency on independent claims 1, 5, 9 and 13 and because they recite subject matter in addition to independent claims 1, 5, 9 and 13; Applicants submit that the dependent claims recite subject matter that is not disclosed or suggested by Erimli; therefore, each of claims 1-15 are not anticipated by Erimli. Examiner respectfully disagrees with these arguments. Erimli et al.

discloses the all claimed features as discussed above. Thus, it is respectfully submitted that the reference of Erimli et al. does anticipate the claimed invention.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kwang B. Yao whose telephone number is 571-272-3182. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KWANG BIN YAO
PRIMARY EXAMINER

Kwang B. Yao
January 11, 2005